

In re: Robert H. Bishop et al.  
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Filed: October 21, 2003  
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### REMARKS

Applicants appreciate the continued thorough examination of the present application that is reflected in the final Official Action of March 3, 2005. Applicants also appreciate the new citation of U.S. Patent 5,269,453 to Melton et al. However, Applicants will now show that the combination of U.S. Patent 5,814,890 to Iwasaki and Melton et al. do not describe or suggest the claimed invention. Accordingly, Applicants respectfully request reconsideration of the outstanding rejections and allowance of the pending claims for the reasons that now will be described.

#### **Independent Claims 8, 14 and 20 Are Patentable Over Iwasaki In View of Melton et al.**

Independent Claim 8 recites:

8. A grid array microelectronic package comprising:  
a substrate;  
an array of external connectors on the substrate that are arranged in at least four rows and at least four columns, including a pair of peripheral rows and a pair of peripheral columns at a periphery thereof and at least one pair of interior rows and at least one pair of interior columns between the respective pair of peripheral rows and peripheral columns, wherein at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are missing from the array to define a routing channel that extends from the periphery of the array towards the interior of the array;  
and  
a plurality of signal conductors that extend from outside the array of external connectors, along the routing channel, and electrically connect to a plurality of the external connectors in an interior row or interior column adjacent the routing channel. (Emphasis added.)

Recitations identical to those underlined above are also contained in remaining independent Claims 14 and 20.

The final Official Action concedes, at the middle of Page 3, that the above recitations are not described or suggested by Iwasaki:

Iwasaki fails to teach a plurality of signal conductors that extend from outside the array of external connectors along the routing channel and electrically connect to a plurality of the external connectors in an interior row or interior column adjacent the routing channel.

In an attempt to supply the missing teachings, the final Official Action now cites Melton et al. The final Official Action contends, at the bottom of Page 3, that:

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Melton et al. teach a grid array package (see Fig. 1-3) having a printed circuit board (PCB-12 in Fig. 1) substrate where a plurality of electrical traces/runners/signal conductors (see 24/20 in Fig. 1-3) along the routing section/channel on the PCB are used to provide the desired electrical connection to respective external connectors (see 30 in Fig. 1-3) in an interior section of an array having external connectors (Col. 2, line 55-Col. 5, line 2). (Emphasis added.)

However, Applicants respectfully submit that Melton et al. appears to be devoid of any teaching of providing a desired electrical connection to respective external connectors in an interior section of an array having external connectors. More specifically, Melton et al. Figure 1 clearly illustrates a bumped integrated circuit die 10 having electrical connections only around its periphery. See, for example, Figure 1, terminal 20, which clearly terminates under the peripheral metal bump 30. Also see Melton et al. Column 2, line 68-Column 3, line 2:

In this embodiment, pads 22 are disposed in a perimeter array pattern for making interconnections about the perimeter of component 10. (Emphasis added.)

Accordingly, Melton et al. does not appear to describe or suggest the claimed electrical connection to external connectors in an interior section of an array, because there simply is no interior section in Melton et al.'s array.

As noted in the present application, for example at Page 6, lines 26-28:

Accordingly, by configuring a routing channel according to embodiments of the present invention, additional access to the interior of the grid array may be provided for routing.

In view of the above, Applicants respectfully submit that neither Iwasaki nor Melton et al. provide any recognition of the problem of allowing additional access to the interior of a grid array, or of the claimed solution that is recited in independent Claims 8, 14 and 20.

Accordingly, independent Claims 8, 14 and 20, and the dependent claims that depend therefrom, are unobvious over Iwasaki in view of Melton et al. Applicants also wish to note that, even if a reference was/is cited that shows the mere formation of a grid array having interior pads, this alone would not describe or suggest the above-underlined recitations of independent Claims 8, 14 and 20.

Independent Claim 14 also is independently patentable. In addition to the recitation of signal conductors described above, Claim 14 also recites:

...wherein at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior

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column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array....

The final Official Action notes at Page 5, that Iwasaki and Melton et al. do not describe or suggest "at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array". In an attempt to supply the missing teaching, U.S. Patent 5,796,169 to Dockerty et al. has been cited, specifically noting the support solder 16 of Figure 3. However, this support solder is placed at corners of the array, as noted by Dockerty et al. Column 4, lines 35-50:

FIG. 3 schematically depicts the ball grid array surface of integrated circuit device 3 according to the present invention, including some refinements thereof. Chevron like, L-shaped support elements, generally at 14, are added to the corner regions of the integrated circuit device ball grid array surface. The support elements are preferably composed of high melting temperature solder, typically the 90/10 lead/tin composition, and extend from each corner along the axes of the ball grid array over multiple solder ball spacing increments. For example, support solder 16 extends over 4 solder spacing increments while support solder 17 extends over three increments. Support solder 18 only extends one solder ball increment in each axial direction while remaining symmetrically within the range of the pattern defined by support solder 16. (Emphasis added.)

Accordingly, Dockerty et al. does not describe or suggest "at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto and electrically strapped together", as recited in the above-quoted recitations of Claim 14. Accordingly, Claim 14 is independently patentable for at least these additional reasons.

Finally, independent Claim 20 also is independently patentable. In particular, the final Official Action has also cited U.S. Patent 6,677,677 to Kimura et al. relative to independent Claim 20. The final Official Action, at the top of Page 7, states that "Kimura et al. teach a GAP having external dummy bumps/external connectors...." Applicants respectfully submit, however, that even if this is the case, Kimura et al. clearly states at Column 2, lines 47-58:

A plurality of bumps comprising the function bumps 2 and the dummy bumps 3 are distributed symmetrically with respect to a center of the semiconductor chip 1. Therefore, even when ultrasonic vibration is applied to the semiconductor chip 1 as in an ultrasonic thermocompression

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bonding method, inconvenience that a portion of the semiconductor chip 1 in which the no function bump 2 exists or a portion of the semiconductor chip 1 where the distribution density of the function bumps 2 is small is largely bent locally is avoided, and the connection force of the function bump 2 is enhanced.

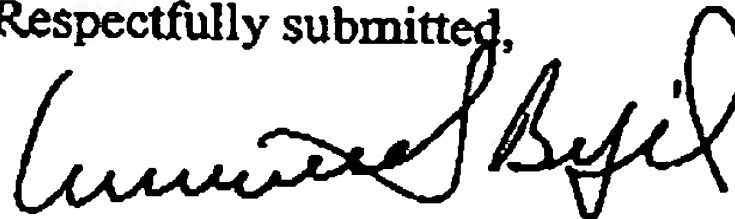
Accordingly, Kimura et al. provides dummy bumps for mechanical considerations, and does not describe or suggest any applicability to routing of connectors. Accordingly, Claim 20 is independently patentable, for at least these additional reasons.

For at least these reasons, independent Claims 8, 14 and 20 are patentable over Iwasaki, Melton et al. and/or Dockerty et al. The pending dependent claims are patentable at least per the patentability of the independent claims from which they depend.

#### Conclusion

Applicants again appreciate the continued thorough examination and the new citation of Melton et al. Applicants have now shown that the cited references do not describe or suggest the recitations of the pending claims. Accordingly, Applicants respectfully request withdrawal of the outstanding rejections and allowance of the present application.

Respectfully submitted,

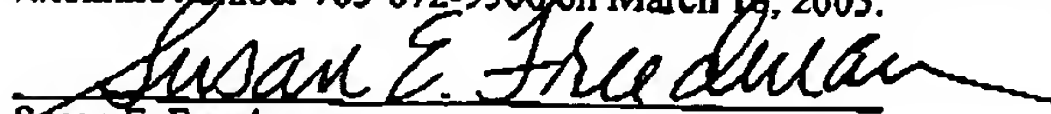


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